WHAT IS CLAIMED:

1. A transceiver couplable to a communications network having a jitter control processor with a transmitter stage, said transmitter stage configured to control a transmit signal, comprising:

a transmit time error measurement system configured to generate a transmit time error signal as a function of timing synchronization associated with a communications network clock and a transceiver master clock;

a transmit filter circuit configured to develop a filtered time error signal as a function of said transmit time error signal; and

a stuffing control system configured to insert a stuffing control signal into said transmit signal as a function of said transmit time error signal and said filtered time error signal.

2. The transmitter stage as recited in Claim 1 further comprising a division counter configured to reduce a communications network clock signal to a transmitter stage frame rate.

3. The transmitter stage as recited in Claim 1 wherein said transmit filter stage comprises a two-input summing node, coefficient elements and a three-input summing node.

4. The transmitter stage as recited in Claim 1 wherein said transmit filter stage comprises a delay element.

5. The transmitter stage as recited in Claim 1 wherein said stuffing control signal includes a maximum of four bits.

6. A method of operating a transceiver couplable to a communications network having a jitter control processor with a transmitter stage, comprising:

generating a transmit time error signal as a function of timing synchronization associated with a communications network clock and a transceiver master clock;

filtering said transmit time error signal to develop a filtered time error signal; and

providing a stuffing control signal into a transmit signal as a function of said transmit time error signal and said filtered time error signal.

7. The method as recited in Claim 6 further comprising reducing a communications network clock signal to a transmitter stage frame rate.

8. The method as recited in Claim 6 wherein said filtering is performed by a transmit filter stage comprising a two-input summing node, coefficient elements and a three-input summing node.

9. The method as recited in Claim 6 wherein said filtering is performed by a transmit filter stage comprising a delay element.

10. The method as recited in Claim 6 wherein said stuffing control signal includes a maximum of four bits.

11. A transceiver couplable to a communications network having a jitter control processor with a receiver stage, said receiver stage, comprising:

a receive time error measurement system configured to generate a receive time error signal as a function of a receive clock signal experiencing jitter and a feedback signal;

a jitter processing circuit configured to develop a dejittered control signal as a function of said time error signal; and

a clock generator system configured to provide said feedback signal as a function of said dejittered control signal and a transceiver local clock signal.

12. The receiver stage as recited in Claim 11 wherein said jitter processing circuit comprises a receive filter stage.

13. The receiver stage as recited in Claim 12 wherein said receive filter stage comprises a summing node and a delay element.

14. The receiver stage as recited in Claim 11 wherein said dejittered control signal comprises a control and offset component.

15. The receiver stage as recited in Claim 11 wherein said clock generator system is configured to provide a dejittered clock signal.

16. A method of operating a transceiver couplable to a communications network having a jitter control processor with a receiver stage, comprising:

generating a receive time error signal as a function of a receive clock signal experiencing jitter and a feedback signal;

developing a dejittered control signal as a function of said time error signal; and

creating said feedback signal as a function of said dejittered control signal and a transceiver local clock signal.

17. The method as recited in Claim 16 wherein said developing is performed by a jitter processing circuit comprising a receive filter stage.

18. The method as recited in Claim 17 wherein said receive filter stage comprises a summing node and a delay element.

19. The method as recited in Claim 16 wherein said dejittered control signal comprises a control and offset component.

20. The method as recited in Claim 16 wherein said creating is performed by a clock generator system that provides a dejittered clock signal.

21. A transceiver coupled to a communications network, comprising:

a system interface that performs system level functions for said transceiver;

a framer that formats signals from said system interface;

a bit pump, coupled to said framer and having a transmit and receive path;

an analog front end, coupled to said bit pump and including a transceiver local clock, that provides a clocking reference for said transceiver; and

a jitter control processor having a transmitter and receiver stage, said transmitter stage configured to control a transmit signal and including:

a transmit time error measurement system that generates a transmit time error signal as a function of timing synchronization associated with a communications network clock and a transceiver master clock,

a transmit filter circuit that develops a filtered time error signal as a function of said transmit time error signal, and

a stuffing control system that inserts a stuffing control signal into said transmit signal as a function of said

transmit time error signal and said filtered time error signal,

said receiver stage, including:

a receive time error measurement system that generates a receive time error signal as a function of a receive clock signal experiencing jitter and a feedback signal,

a jitter processing circuit that develops a dejittered control signal as a function of said time error signal, and

a clock generator system that provides said feedback signal as a function of said dejittered control signal and said transceiver local clock signal.

22. The transceiver as recited in Claim 21 wherein said transmitter stage further comprises a division counter that reduces a communications network clock signal to a transmitter stage frame rate.

23. The transceiver as recited in Claim 21 wherein said transmit filter stage comprises a two-input summing node, coefficient elements and a three-input summing node.

24. The transceiver as recited in Claim 21 wherein said transmit filter stage comprises a delay element.

25. The transceiver as recited in Claim 21 wherein said stuffing control signal includes a maximum of four bits.

26. The transceiver as recited in Claim 21 wherein said jitter processing circuit comprises a receive filter stage.

27. The transceiver as recited in Claim 26 wherein said receive filter stage comprises a summing node and a delay element.

28. The transceiver as recited in Claim 21 wherein said dejittered control signal comprises a control and offset component.

29. The transceiver as recited in Claim 21 wherein said clock generator system provides a dejittered clock signal.